FIG. 1

DIAGRAM OF CONSTRUCTION OF EMBODIMENT

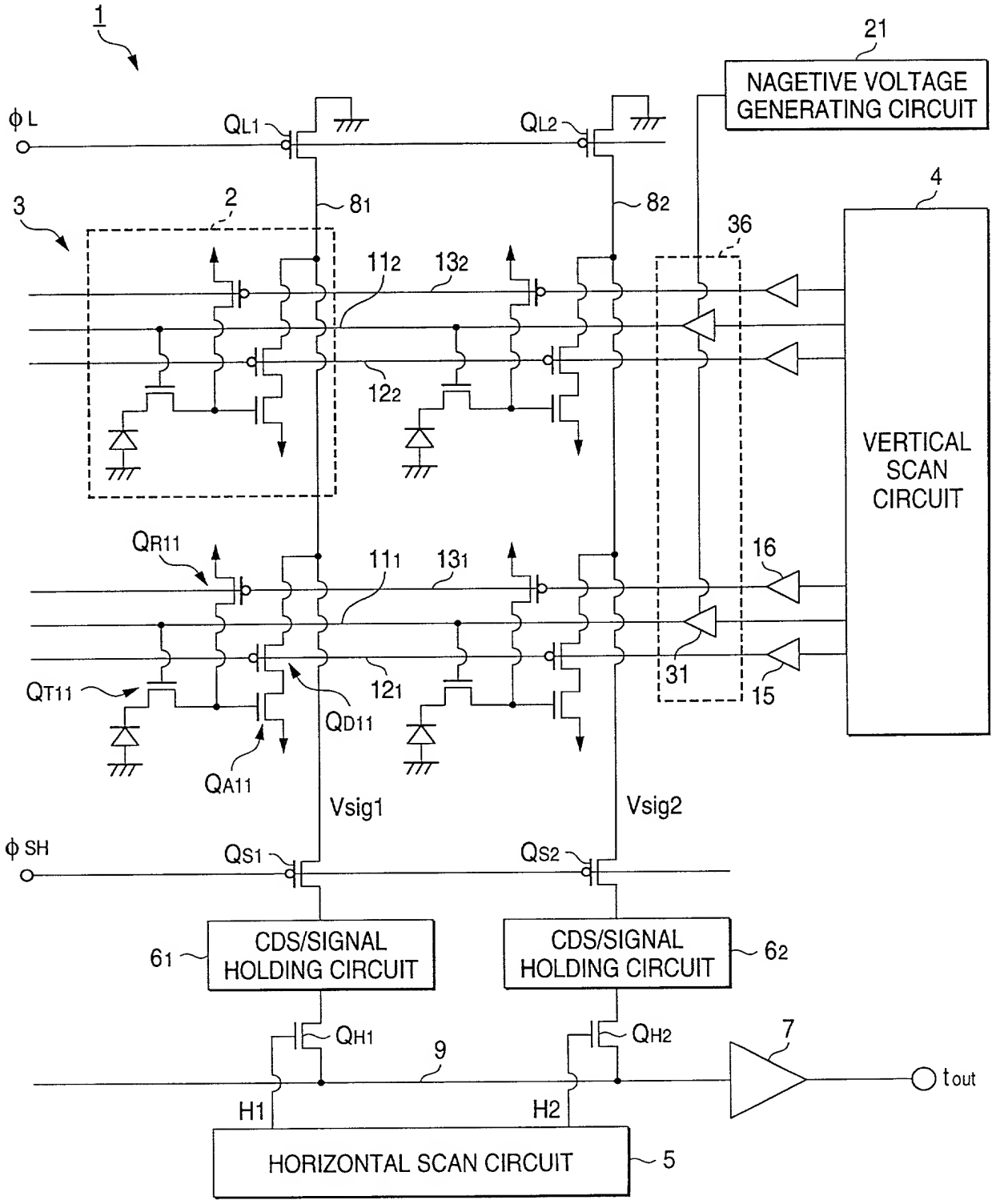


FIG. 2

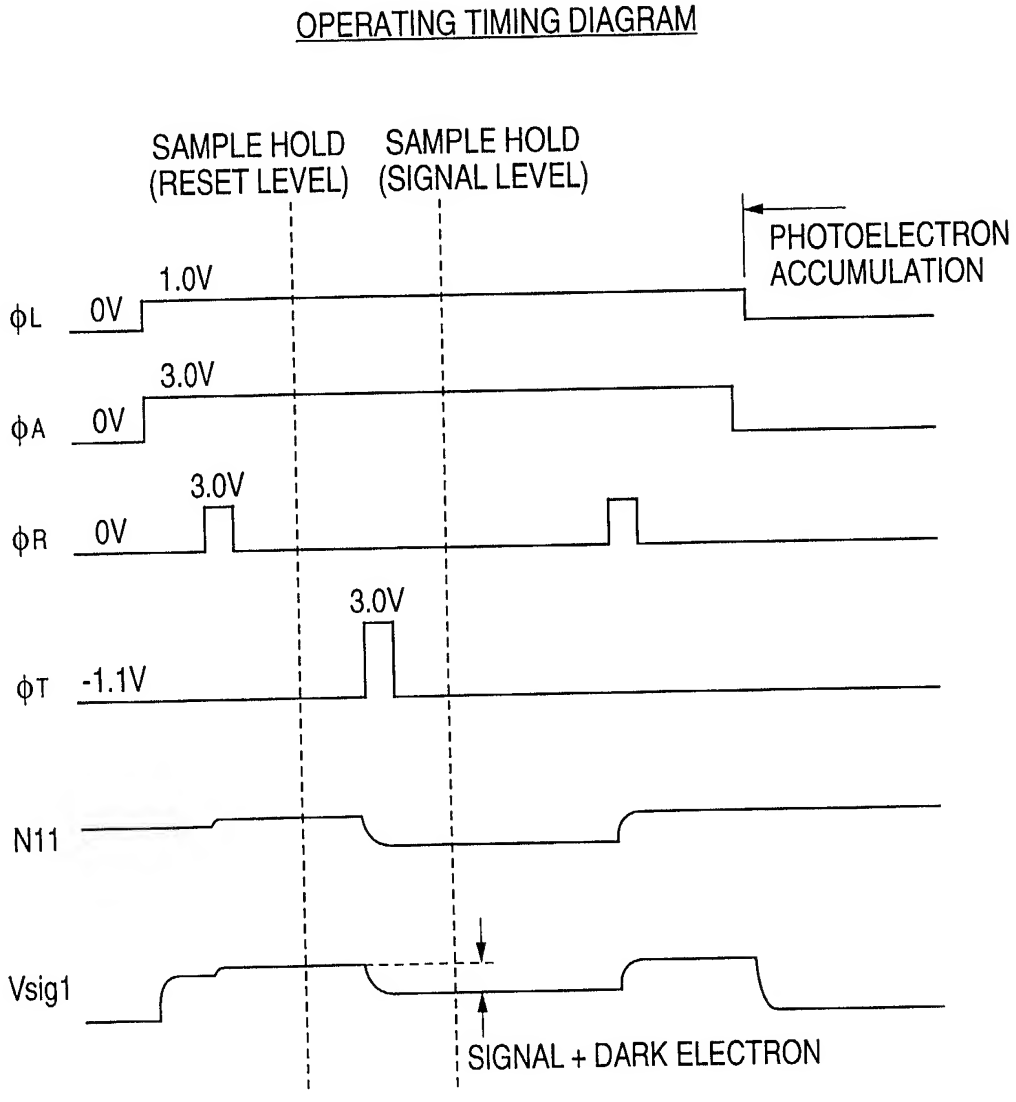

OPERATING TIMING DIAGRAM
SAMPLE HOLD (RESET LEVEL)
SAMPLE HOLD (SIGNAL LEVEL)
PHOTOELECTRON ACCUMULATION
ϕL
1.0V
0V
ϕA
3.0V
0V
ϕR
3.0V
0V
ϕT
3.0V
-1.1V
N11
Vsig1
SIGNAL + DARK ELECTRON

FIG. 3

EXAMPLE OF BUFFER CIRCUIT (15, 16)

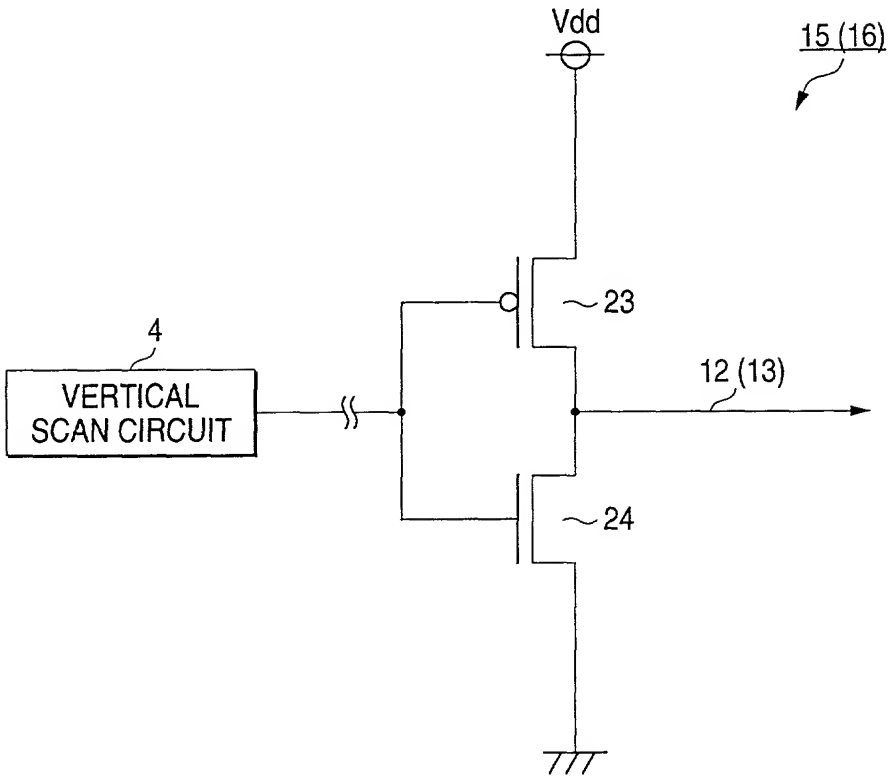


FIG. 4

EXAMPLE OF BUFFER CIRCUIT (31)

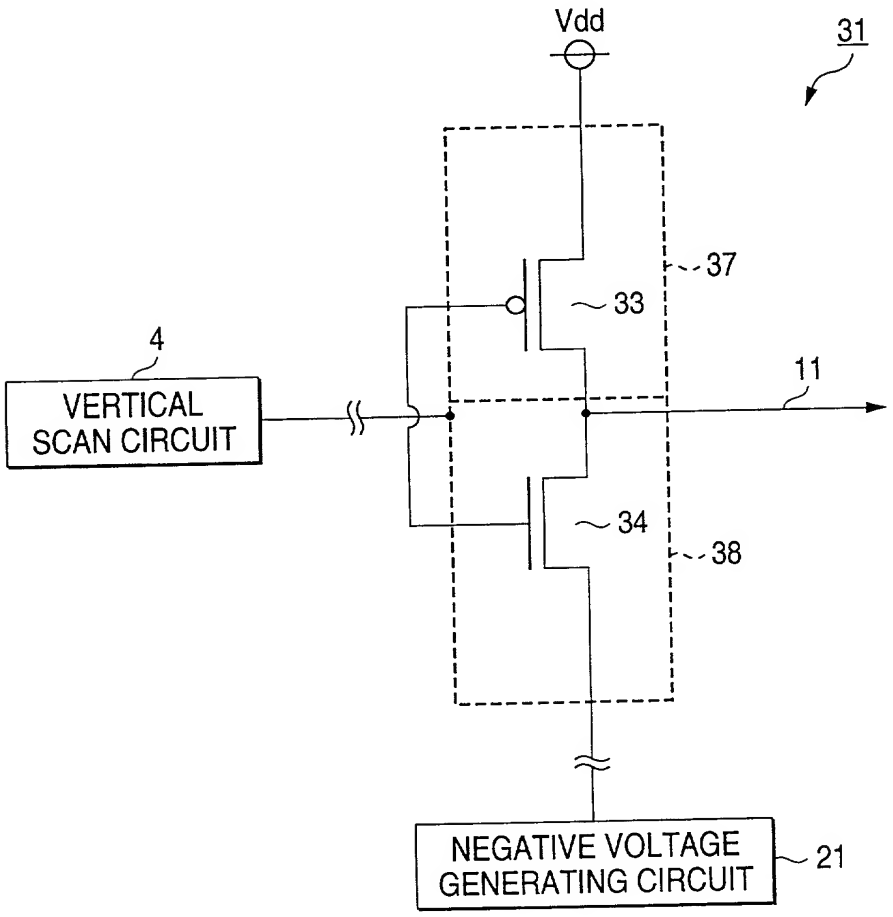


FIG. 5

CROSS-SECTIONAL VIEW OF PHOTODIODE AND TRANSFER TRANSISTOR OF FIRST EMBODIMENT

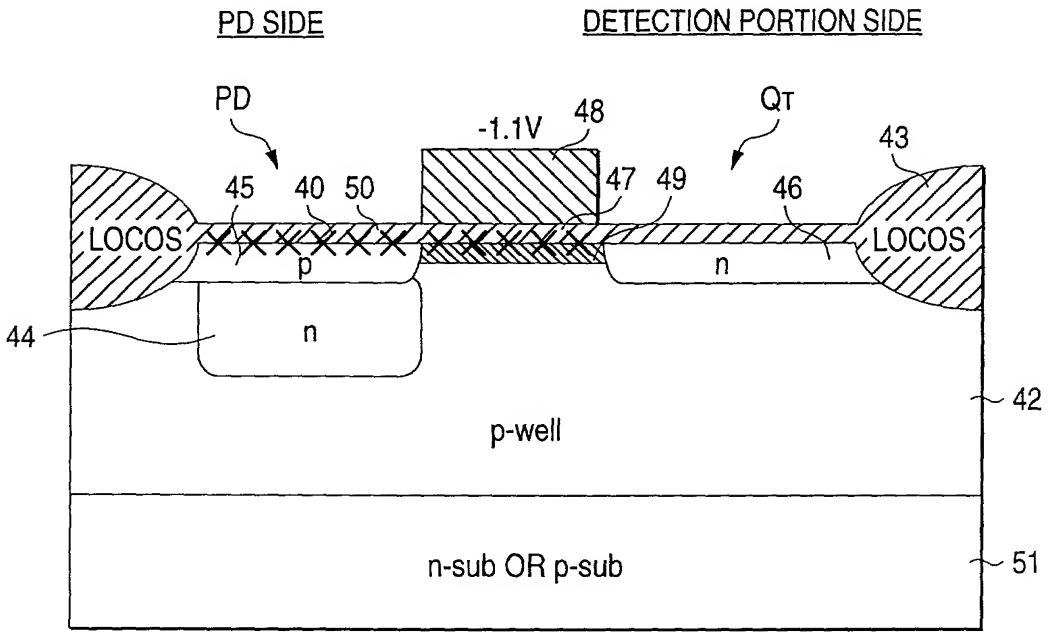


FIG. 6

CROSS-SECTIONAL VIEW OF PHOTODIODE AND TRANSFER TRANSISTOR OF SECOND EMBODIMENT

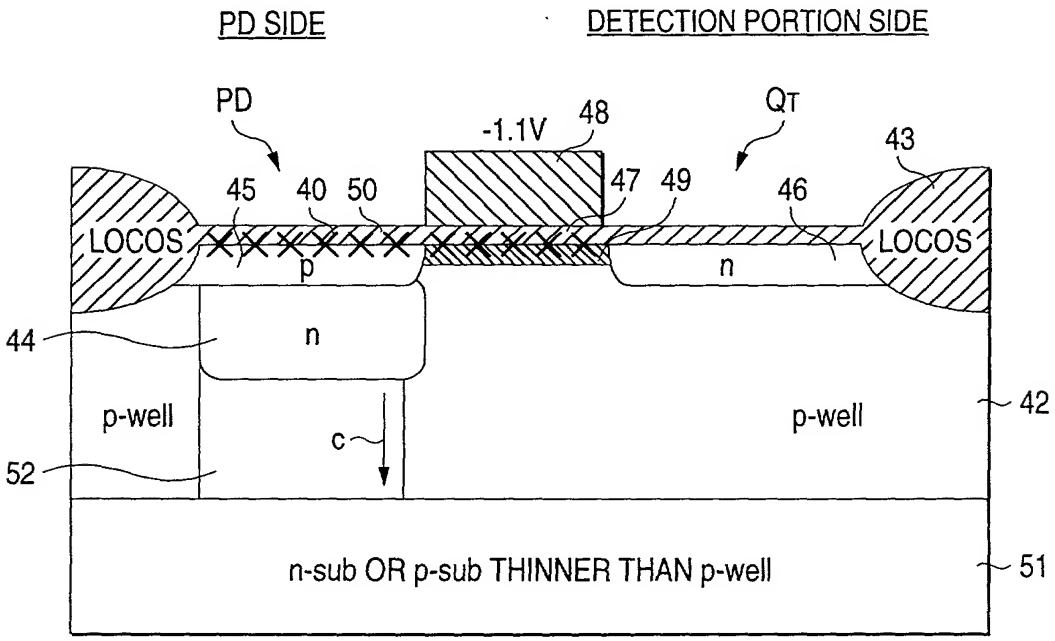


FIG. 7

CROSS-SECTIONAL VIEW OF PHOTODIODE AND TRANSFER TRANSISTOR OF THIRD EMBODIMENT

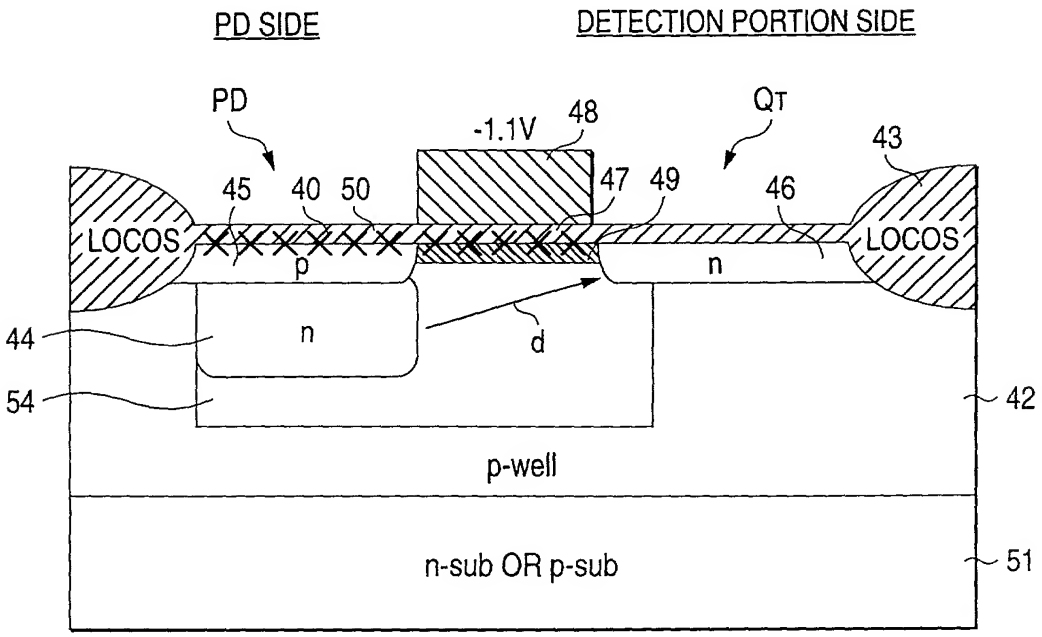


FIG. 8

CROSS-SECTIONAL VIEW OF PHOTODIODE AND TRANSFER TRANSISTOR OF FOURTH EMBODIMENT

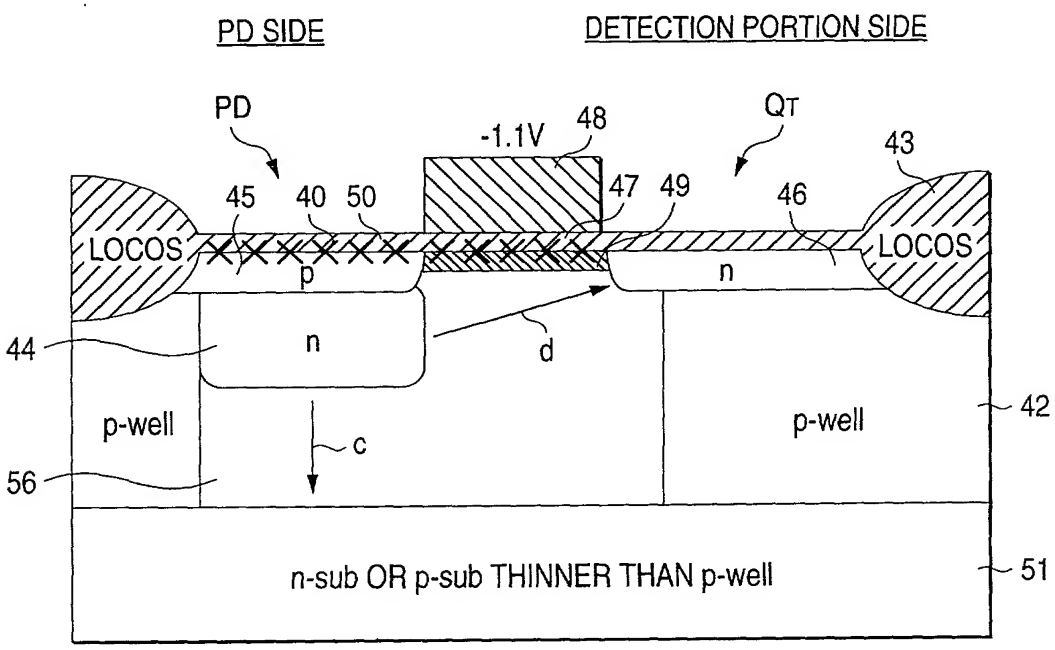


FIG. 9

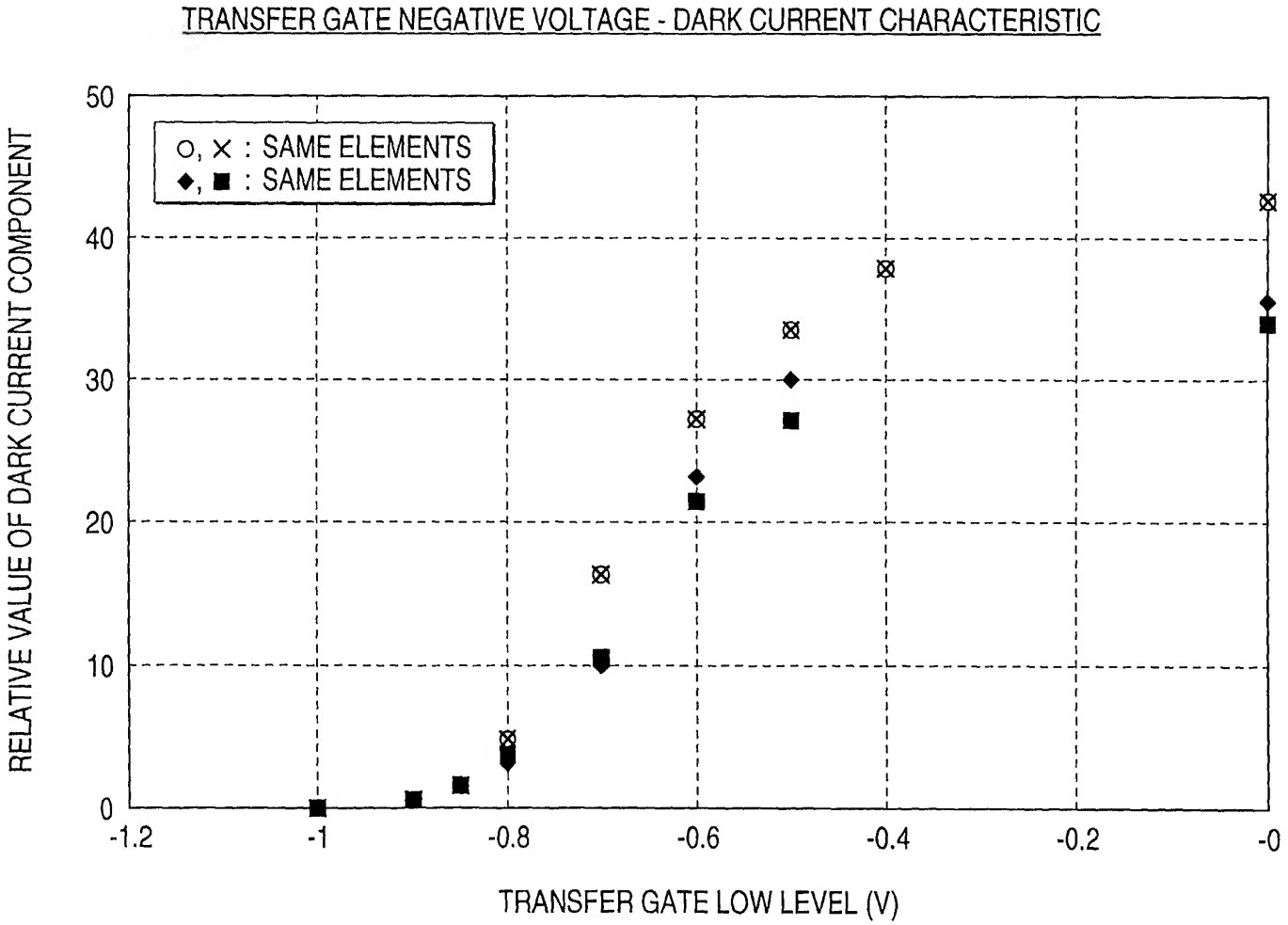
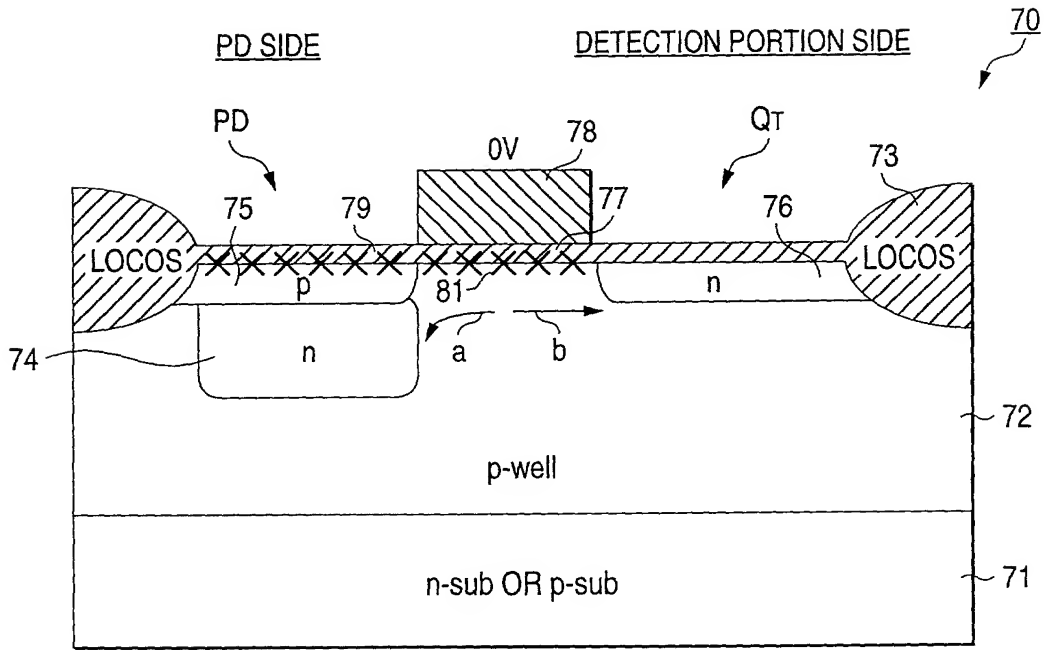

TRANSFER GATE NEGATIVE VOLTAGE - DARK CURRENT CHARACTERISTIC
○, × : SAME ELEMENTS
◆, ■ : SAME ELEMENTS
RELATIVE VALUE OF DARK CURRENT COMPONENT
50
40
30
20
10
0
-1.2
-1
-0.8
-0.6
-0.4
-0.2
-0
TRANSFER GATE LOW LEVEL (V)

FIG. 10

DIAGRAM OF DEVICE OF DARK CURRENT



× : DEFECTS OF INTERFACE

FIG. 11

CROSS-SECTIONAL VIEW OF PRIOR ART